



E.E. 451.3

**VLSI Circuit Design**

**Instructor: R.J. Bolton**

**MID-TERM EXAMINATION**

February 15, 2001

8:30 AM - 9:30 AM

STUDENT NAME: \_\_\_\_\_

STUDENT NUMBER: \_\_\_\_\_

Question 1	/ 15
Question 2	/ 15
Question 3	/ 15
TOTAL	/ 45

**GENERAL INSTRUCTIONS FOR THE QUESTIONS**

- 1) OPEN E.E. 451.3 textbook (**Principles of CMOS VLSI Design - A Systems Perspective by N.H.E. Weste and K. Eshraghian OR one other text**), OPEN E.E. 451.3 notes, and OPEN E.E. 451.3 assignments.
- 2) NO library manuals (or copies thereof) ALLOWED! NO examination files ALLOWED!
- 3) Neatness counts. Please ensure your paper is readable.
- 4) Some questions contain special instructions. Please ensure that you read these carefully.
- 5) Not all questions are of the same difficulty and value. Consider this when allocating time for the solution.
- 6) **IF A QUESTION PROVES TO BE TOO HARD FOR YOU TO SOLVE, GO ON TO ANOTHER QUESTION! RETURN TO THE TROUBLESONE QUESTION WHEN TIME PERMITS.**

**PLEASE NOTE**

**ALL parts of the examination paper MUST be handed in before leaving.**

**Please check that your examination paper contains 7 pages TOTAL.**

### SPECIFIC INSTRUCTIONS FOR THE EXAMINATION

- 1) All designs use standard CMOS3DLM design rules and layers.  $V_{DD} = +5V$  and  $V_{SS} = 0V$ .
- 2) Unless otherwise specified, normal substrate connections are assumed for all P-channel and N-channel transistors, i.e.,  $V_{SS}$  for N-channel and  $V_{DD}$  for P-channel.
- 3) CMOS3DLM resistance and capacitance parameters are as follows:

Layer	Resistance	Capacitance
N-Diffusion	25.0 $\Omega/\square$	4.4E-4 $\text{pf}/\mu\text{m}^2$
P-Diffusion	80.0 $\Omega/\square$	1.5E-4 $\text{pf}/\mu\text{m}^2$
Polysilicon	18.0 $\Omega/\square$	6.0E-5 $\text{pf}/\mu\text{m}^2$
Metal 1	0.035 $\Omega/\square$	2.7E-5 $\text{pf}/\mu\text{m}^2$
Metal 2	0.030 $\Omega/\square$	1.4E-5 $\text{pf}/\mu\text{m}^2$
N-Transistor	4275 $\Omega/\square$	See below
P-Transistor	13600 $\Omega/\square$	See below
Gate-channel	See above	6.9E-4 $\text{pf}/\mu\text{m}^2$

- 4) Supplementary physical constants are as follows:

Constant	Symbol	Value	Units
Electron charge	$q$	1.602E-19	coulomb
Boltzmann's constant	$k$	1.38E-23	Joule/ $^\circ\text{K}$
Intrinsic carrier concentration of Si @ T=300 $^\circ\text{K}$ (27 $^\circ\text{C}$ )	$n_i^2$	2.1E+20	(carriers/cm $^3$ ) $^2$
Permittivity of free space	$\epsilon_0$	8.854E-14	Farad/cm
Permittivity of Si	$\epsilon_s$	11.7 $\epsilon_0$	Farad/cm
Permittivity of $\text{SiO}_2$	$\epsilon_{ox}$	3.9 $\epsilon_0$	Farad/cm

- 5) (H)SPICE process parameters are as follows:

Parameter	Name	N-channel	P-channel	Units
$V_t$	Zero-bias threshold voltage	0.7	-0.8	Volts
$\kappa'$	Process gain factor	40.0E-6	12.0E-6	A/V $^2$
$\gamma$	Bulk threshold body factor	1.1	0.6	V $^{1/2}$
$2  \phi $	Surface potential	0.6	0.6	V
$\lambda$	Channel length modulation factor	1.0E-2	3.0E-2	1/V
$t_{ox}$	Oxide thickness	5.0E-6	5.0E-6	cm
$N_A$ or $N_D$	Substrate doping density	1.7E+16	5.0E+15	1/cm $^3$
$\mu$	Carrier surface mobility	775	250	cm $^2$ /(V·sec)

**QUESTION #1****MARKS: 15 (3 + 3 + 3 + 3 + 3)**

Indicate (in the space provided) whether the following are TRUE or FALSE. Do any FIVE (5). To obtain full marks for each question, include a SHORT sentence or two in support of your answer.

- F 1) Minimum spacing design rules are needed to account for mask alignment errors.

MINIMUM SPACING RULES ARE FOR GEOMETRY ON  
SAME LAYER. THEREFORE ONLY ONE MASK IS  
INVOLVED.

- F 2) A layout in which the designer uses all of the bonding pads is said to be "metal-limited".

METAL-LIMITED DESIGNS ARE ONES IN WHICH  
THE DESIGNER RUNS OUT OF SPACE TO RUN  
METAL INTERCONNECT.

- T 3) Most sequential circuits use multi-phase non-overlapping clocks.

WHILE THEY MAY USE A SINGLE PHASE  
GLOBAL CLOCK, WE USE TWO PHASE NON-  
OVERLAPPING CLOCKS LOCALLY.

- F 4) The Canadian Microelectronics Corporation (CMC) does fabrication for the U of S.

THE CMC DOES NOT DO FABRICATION.

- T 5) Most modern CMOS technologies are "self-aligned".

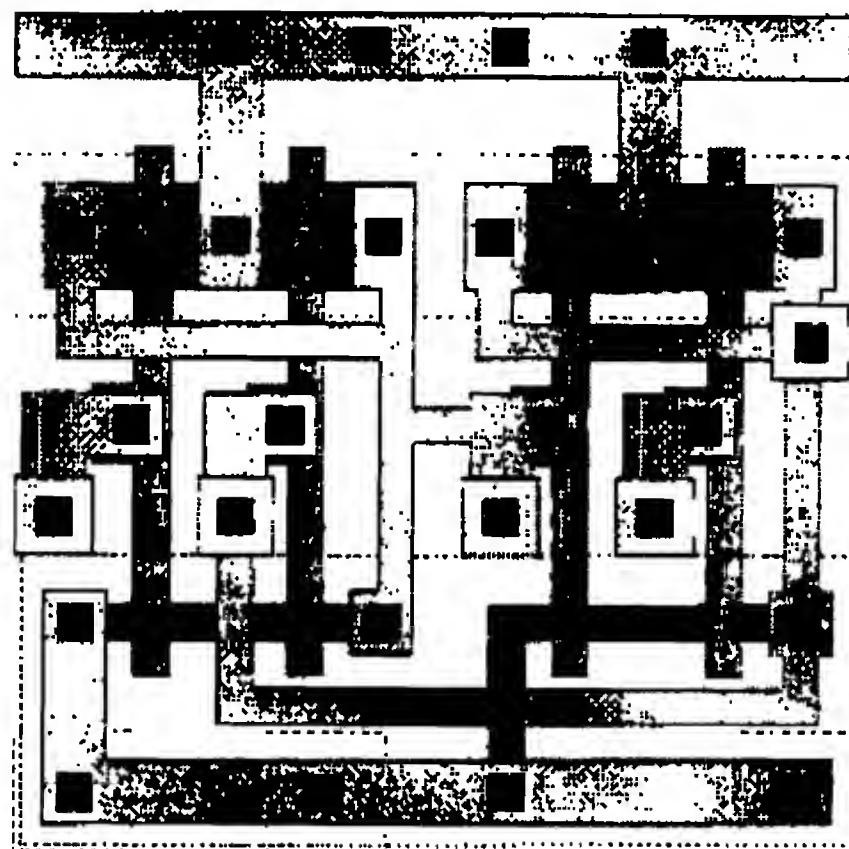
THEY ARE CALLED "SELF-ALIGNED" SINCE THE  
GATE (POLYSILICON) IS USED AS A MASK FOR  
THE SOURCE AND DRAIN DIFFUSIONS.

- F 6) Sputtering is the process by which photoresists are deposited on the surface of an wafer.

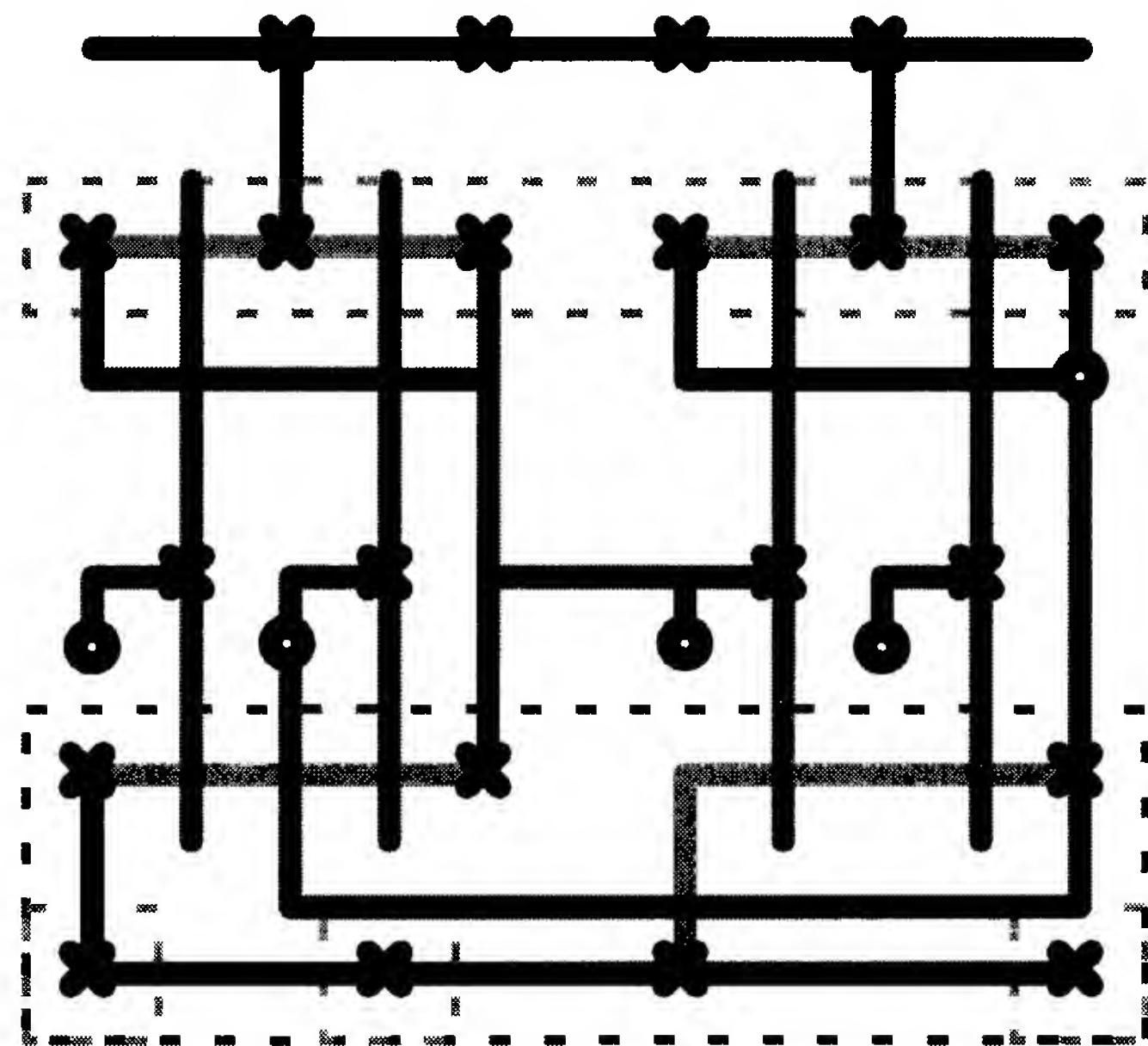
SPUTTERING IS USED TO DEPOSIT METAL.

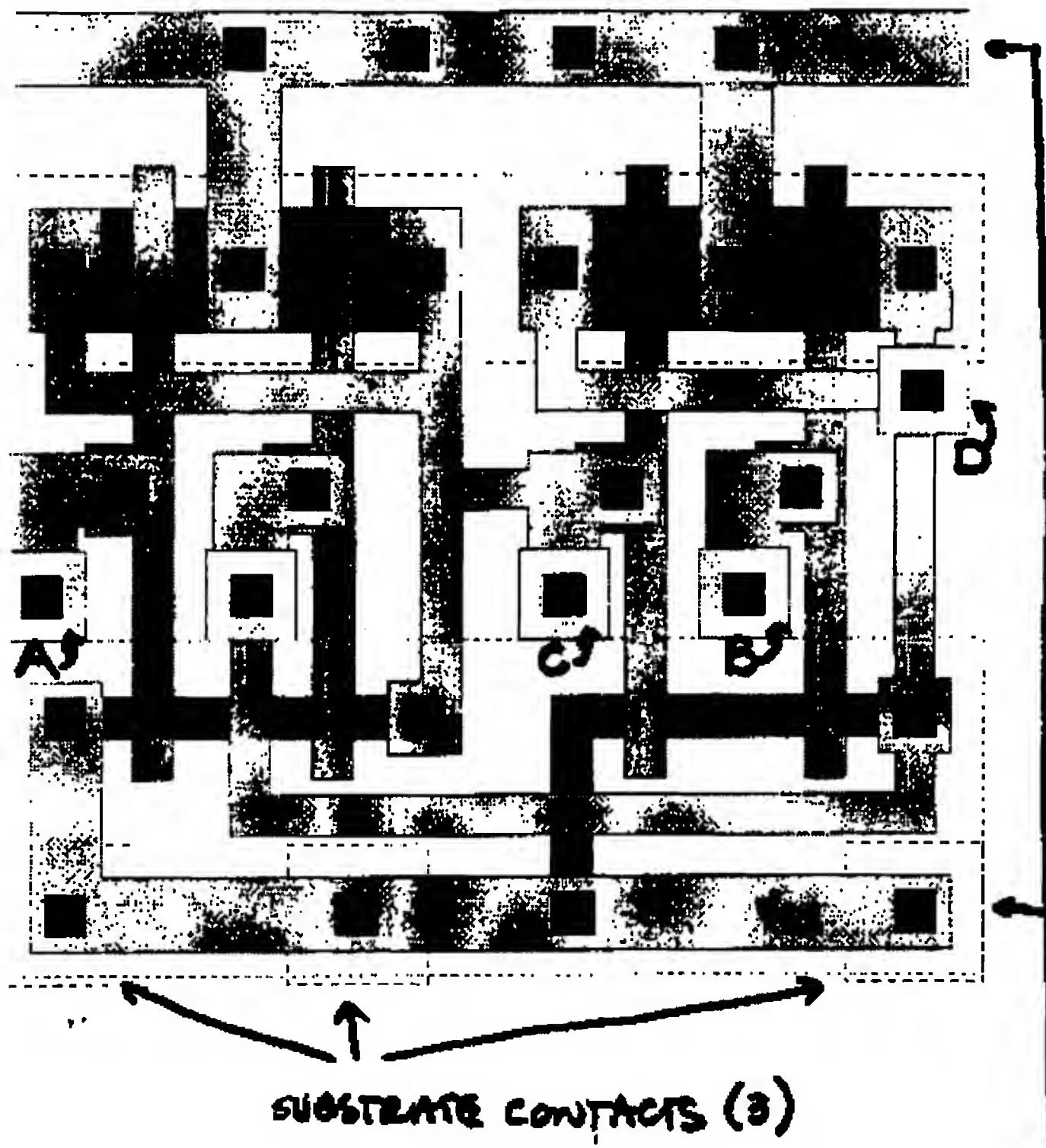
**QUESTION #2****MARKS: 15 (5 + 5 + 4 + 1)**

Consider the following plot of a CMOS3DLM circuit shown below (and on the following page).



- a) Determine the function of the circuit. Do this by drawing a STICKS diagram of the circuit and a gate-level schematic of the circuit. Use the next page. When drawing the STICKS diagram use standard E.E. 451.3 colors (see next page):
- b) Indicate each of the following:
- SEQUENTIAL Combinational or Sequential?
  - 3 dsm Width of the power supply lines ( $V_{DD}$  and  $V_{SS}$ )?
  - 0 Number of Transmission gates?
  - 2 Number of Output ports?
  - 3 Number of N-channel transistor P-Well substrate contacts?
- c) Estimate the height of the circuit. Assume circuit layout is in design scale microns (dsm). Use metal and metal2 width, spacing and enclosure to determine height (go up left and left center of layout)
- $$H = 4 + 9 + 5 + 5 + 5 + 9 + 5 + 11 + 3 + 9 + 5 + 5 + 5 + 15 + 15 + 9 = 119 \text{ dsm}.$$
- ↑  
 STUFF BELOW       $w = \text{WIDTH}$        $cc = \text{CONTACT CUT}$   
 $V_{SS}$        $s = \text{SPACING}$        $v = \text{VIA}$
- d) If you had to (easily) reduce the area of the CMOS3DLM circuit layout, what single thing would you do?
- MOVE THE TOP  $V_{DD}$  POWER RAIL DOWN  $\approx 10 \text{ dsm}$ .



Question #2 Work Sheet

SUBSTRATE CONTACTS (3)

CMOS3DLM Layer	Color
N+ diffusion	Green
P+ diffusion	Orange
P+ mask	Dotted Orange
Polysilicon	Red
P-Well	Dotted Brown
Metal 1	Blue
Metal 2	Black or Purple
Contact Cut	Black X
Via	Black O

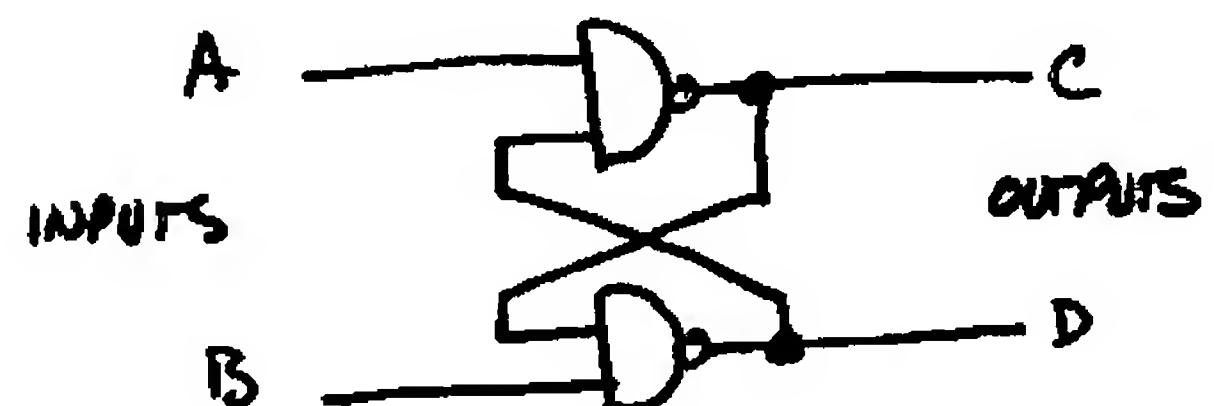
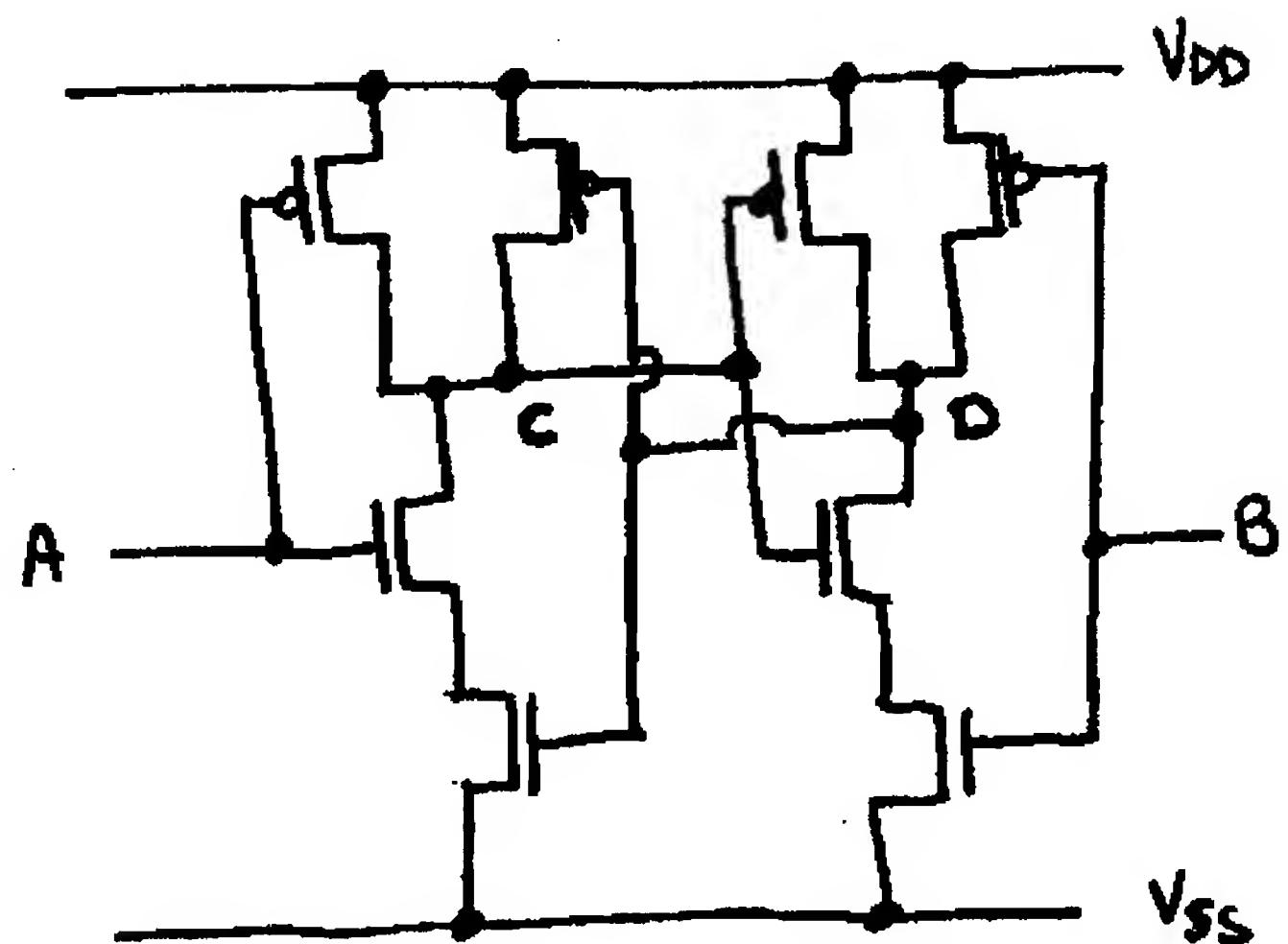
Please note that the circuit layout shown on the left contains all of the layers in the table above.

$V_{DD} = 90\text{m}$   
 $V_{SS} = 90\text{m}$

SEE LAST PAGE FOR  
STICKS DIAGRAM.

THERE ARE NO TRANSMISSION  
GATES IN THIS DESIGN.

CIRCUIT IS A RS FLIP-FLOP.  
MADE FROM NAND GATES.



$A + B$ : INPUTS

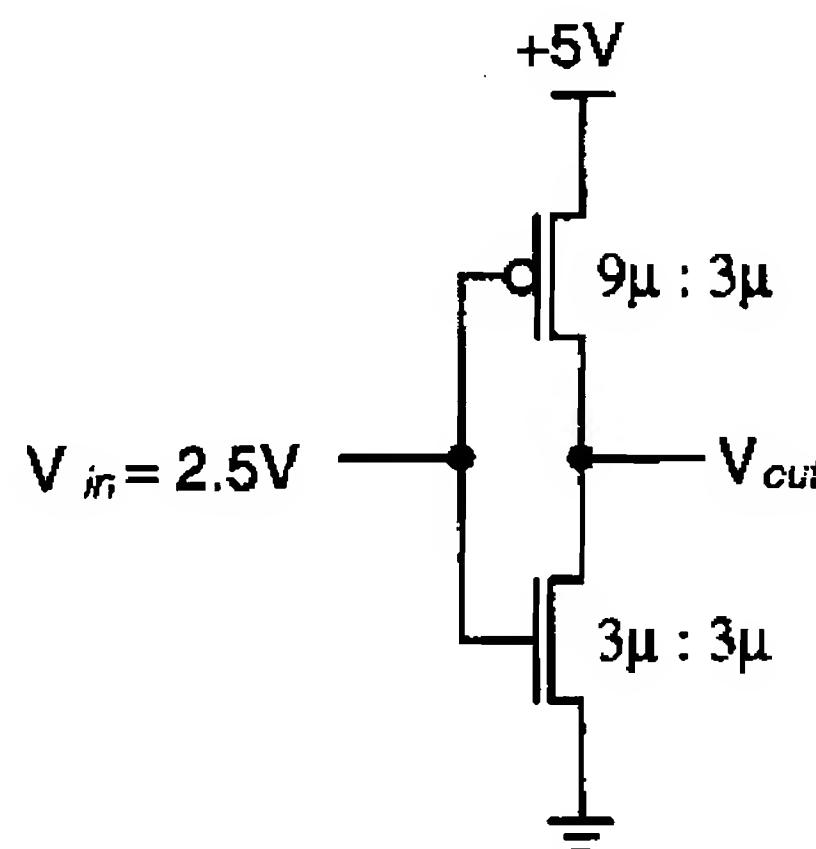
$C + D$ : OUTPUTS

QUESTION #3

MARKS: 15 (15)

- a) The following circuit is one of many standard designs for a CMOS DLM inverter. Calculate the current,  $I_{DS}$ , from  $V_{DD}$  to  $V_{SS}$  when the input voltage,  $V_{in}$ , is 2.5V. Important parameters are shown on Page 2. Show your calculation. Sizes shown are W:L.

You must state any assumption(s) that you make.



$$\beta_n = 53.5 \mu A/V^2 \left( \frac{W}{L} \right) = 53.5 \mu A/V^2 \quad \beta_p = 17.3 \mu A/V^2 \left( \frac{W}{L} \right) = 51.9 \mu A/V^2$$

Since  $\frac{\beta_n}{\beta_p} > 1$   $V_{out}$  vs  $V_{in}$  curve (from ASSIGNMENT #1)

MOVES TO THE LEFT. THEREFORE WE ARE IN REGION D

(N-CHEMICAL NON-SATURATED AND P-CHEMICAL SATURATED).

$$\begin{aligned} \therefore |I_{DSp}| &= \left| -\frac{\beta_p}{2} (V_{in} - V_{DD} - V_{TP})^2 \right| \\ &= \left| -\frac{51.9 \mu A/V^2}{2} (2.5 - 5 + 0.8)^2 \right| \\ &= \underline{\underline{75 \mu A}} \end{aligned}$$

NOTE: BECAUSE  $\beta_n \neq \beta_p$  AND  $V_{in} \neq V_{TP}$  IT IS NOT SAFE TO ASSUME BOTH TRANSISTORS ARE IN SATURATION. IN FACT  $V_{out}$  IS EQUAL TO 1.3V. THIS IS DUE TO STEEP SLOPE IN  $V_{out}$  VS  $V_{in}$  CURVE.

(CHECKED WITH WINSPIRE:  $|I_{DS}| = 69.2 \mu A \quad V_{out} = 1.02V$ )